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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,651	ADAMS ET AL.	
	Examiner	Art Unit	
	PHUNG My CHUNG	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 16-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims is withdrawn in view of the newly discovered reference(s) to Schwarz (6,795,942). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-14, 16-21, 23, 25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarz (6,795,942).

As per claims 16, Schwarz discloses an apparatus comprising:

a memory having a plurality of memory elements (columns or rows);

a redundant memory element (redundant column or redundant row) suitable for replacing at least one of the plurality of memory elements;

a self-test circuit (BIST) that tests the memory and allocates the redundant memory element to one of the plurality of memory elements if a defect is found, the self-test circuit including a multiplexer that selectively couples memory outputs to a fault counter that counts fails in each one of the plurality of memory elements tested by the self-test circuit. (See col. 2, lines 40-67 and col. 3, lines 1-3). Schwarz further discloses a compare circuit that compares the number of fails in each of the memory elements with a defect threshold (col. 5, lines 4-8, lines 15-16, and lines 44-49). Schwarz does

not specifically disclose recording the memory element having the most fails. However, Schwarz, col. 2, lines 20-22, lines 40-55 and col. 12, lines17-21, discloses record the number and location of each defective element before the tester can execute its repair algorithm. If the number of defects in any element exceeds a threshold value, that element is flagged for replacement by one of the redundant elements (col. 5, lines 15-16, the most defects are the first to be replaced) and col. 11, lines 38-39). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, base on the comparison circuit that compares the number of fails in each of the memory elements with a defect threshold and record the number and location of each defective element before the tester can execute its repair algorithm as taught by Schwarz to set the comparison circuit to compare the number of fails in each of the memory elements with each other and record only the element that having the most fails so that only the most fail element can be recorded for later repair, thereby constitute a cost-effective and improving memory device yields.

As per claim 17, Schwarz further discloses a fault count storage that stores numbers of fails and address information for one or more memory elements containing fails detected during a self-test. (See col. 2, lines 20-22 and lines 40-55 and col. 5, lines 15-16).

As per claim 18, Schwarz further discloses wherein the plurality of memory elements include at least one of a row, a column, or an input/output. (See col. 5, lines 25-26).

As per claim 19, Schwarz further discloses a second fault counter that counts fails in a second plurality of memory elements (col. 9, lines 11-17).

As per claim 20, Schwarz further discloses a reset signal provided to the fault counter after testing of each memory element (col. 9, line 67 to col. 10 lines 1-3).

As per claim 21, Schwarz further discloses wherein the self-test circuit allocates one or more redundant rows after allocating at least one of redundant columns or redundant input/outputs. (See col. 5, lines 21-61).

As per claims 1-4, 6, these method claims are rejected under similar rationale as set forth in claim 16.

As per claim 5, Schwarz further disclose wherein the memory is identified as un-repairable when the number of memory elements having fails exceeds the number of redundant memory elements (col. 6, line 38-42).

As per claims 7-9 and 11, these method claims are rejected under similar rationale as set forth in claim 18.

As per claims 10 and 12, these method claims are rejected under similar rationale as set forth in the system claim 19.

As per claim 13, this method claim is rejected under similar rationale as set forth in claim 1.

As per claim 23, this apparatus claim is rejected under similar rationale as set forth in claim 16.

As per claim 25, Schwarz further discloses wherein the self-test provides a reset signal to the counter after testing each one of the plurality of memory elements (col. 9, line 67 to col. 10 lines 1-3).

As per claims 27-29, these claims are rejected under similar rationale as set forth in claim 17.

4. Claims 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarz (6,795,942) as applied to claims 16 and 23 above, and further in view of Nadeau-Dostie et al (6,738,938).

Claims 22 and 24, the teaching of Schwarz has been discussed above. Schwarz does not disclose an embedded memory of an integrated circuit and that the fault detection circuit that compares output to an expected memory output. However, Nadeau-Dostie et al disclose a memory can be embedded in the integrated circuit (see col. 2, line 66) and a BIST further includes a data comparator for comparing output data received from the integrated circuit with expected output data (col. 1, lines 19-26). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the embedded memory in the integrated circuit and the comparator that compares output data received from the integrated circuit with expected output data as taught by Nadeau-Dostie et al into the BIST of Schwarz to detect failure within the integrated circuit when the output data received from the integrated circuit differs from the expected output data.

5. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarz (6,795,942) as applied to claims 16 and 23 above, and further in view of the applicant admitted prior art (hereafter referred to as the AAPA).

As per claim 24, the teaching of Schwarz has been discussed above. Schwarz does not specifically disclose that the fault detection circuitry includes an exclusive-OR logic gate that compares a memory output to an expected memory output. However, the AAPA, Fig. 2, block 120 is an exclusive-OR logic gate that compares a memory output to an expected memory output. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the exclusive-OR logic gate that compares a memory output to an expected memory output as taught by the AAPA into the error detection circuit of Schwarz to detect error when the expected memory output differs from the memory output.

As per claim 26, Schwarz further discloses wherein the self-test provides a reset signal to the counter after testing each one of the plurality of memory elements (col. 9, line 67 to col. 10 lines 1-3).

6. Applicant's arguments with respect to claims 1-14 and 16-29 have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUNG My CHUNG whose telephone number is (571)272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phung My Chung/

Primary Examiner, Art Unit 2117